

NE

NE

SR

NNN	NNN	EEEEEEEEE	TTTTTTTTT	AAAAAAA	CCCCCCC	PPPPPPP
NNN	NNN	EEEEEEEEE	TTTTTTT	AAAAAAA	CCCCCCC	PPPPPPP
NNN	NNN	EEEEEEEEE	TTTTTTT	AAAAAAA	CCCCCCC	PPPPPPP
NNN	NNN	EEE	TTT	AAA	CCC	PPP
NNN	NNN	EEE	TTT	AAA	CCC	PPP
NNN	NNN	EEE	TTT	AAA	CCC	PPP
NNNNNN	NNN	EEE	TTT	AAA	CCC	PPP
NNNNNN	NNN	EEE	TTT	AAA	CCC	PPP
NNNNNN	NNN	EEE	TTT	AAA	CCC	PPP
NNNNNN	NNN	EEE	TTT	AAA	CCC	PPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCC	PPPPPPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCC	PPPPPPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCC	PPPPPPP
NNN NNNNN	NNNN	EEE	TTT	AAAAAAA	CCC	PPP
NNN NNNNN	NNNN	EEE	TTT	AAAAAAA	CCC	PPP
NNN NNNNN	NNNN	EEE	TTT	AAAAAAA	CCC	PPP
NNN NNN	NNN	EEE	TTT	AAA	CCC	PPP
NNN NNN	NNN	EEE	TTT	AAA	CCC	PPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCCCCCC	PPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCCCCCC	PPP
NNN NNN	NNN	EEEEEEEEE	TTT	AAA	CCCCCCC	PPP

FILEID**NETDRVQRL

L 9

NN NN EEEEEEEEEE TTTTTTTTTT DDDDDDDDD RRRRRRRRR VV VV QQQQQQ RRRRRRRR LL
NN NN EEEEEEEEEE TTTTTTTTTT DDDDDDDDD RRRRRRRRR VV VV QQQQQQ RRRRRRRR LL
NN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NNNN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NNNN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NN NN EEEEEEEEEE TT DD DD RRRRRRRR VV VV QQ QQ RRRRRRRR LL
NN NN NN EEEEEEEEEE TT DD DD RRRRRRRR VV VV QQ QQ RRRRRRRR LL
NN NNNN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NNNN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NN EE TT DD DD RR RR VV VV QQ QQ RR RR LL
NN NN EEEEEEEEEE TT DDDDDDDDD RR RR VV VV QQQQ QO RR RR LLLLLLLLLL
NN NN EEEEEEEEEE TT DDDDDDDDD RR RR VV VV QQQQ QO RR RR LLLLLLLLLL

....
....
....

LL IIIII SSSSSSS
LL IIIII SSSSSSS
LL II SS
LL II SS
LL II SS
LL II SSSSS
LL II SSSSS
LL II SS
LL II SS
LL II SS
LL II SS
LL LLLLLLLL IIIII SSSSSSS
LL LLLLLLLL IIIII SSSSSSS

(2)	44	MODIFICATION HISTORY
(3)	56	DECLARATIONS
(6)	122	QRL\$SOLICIT - Process ECL request to xmit into the network
(7)	180	QRL\$DENY - Deny solicitor permission to transmit
(7)	181	QRL\$GRANT - Grant solicitor permission to transmit
(11)	466	QRL\$SETUP_CHAN - Setup channel to specified node
(12)	552	QRL\$SETUP_RTHDR - Build route-header
(13)	666	QRL\$SETUP_X_IRP - Allocate, init, queue IRP

0000 1 :& - Someday, the LPE will be supported as part of the LPD
0000 2
0000 3 .TITLE NETDRVQRL - DECnet 'Quick Routing Layer' module for NETDRIVER
0000 4 :IDENT 'V04-000'
0000 5 :*****
0000 6 :*****
0000 7 :*
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0000 25 :*
0000 26 :*
0000 27 :*****
0000 28
0000 29 :++
0000 30 :FACILITY: DECnet, Executive
0000 31
0000 32 :ABSTRACT:
0000 33 : This module implements a quick interface for high speed
0000 34 : communications in end-node environments where the partner
0000 35 : node is 1-hop away, e.g., Ethernet environments. The
0000 36 : motivation for it is the inordinate amount of time spent in
0000 37 : the more general purpose NETDRVXPT module.
0000 38
0000 39 : ENVIRONMENT: Standard driver environment
0000 40
0000 41 :--
0000 42

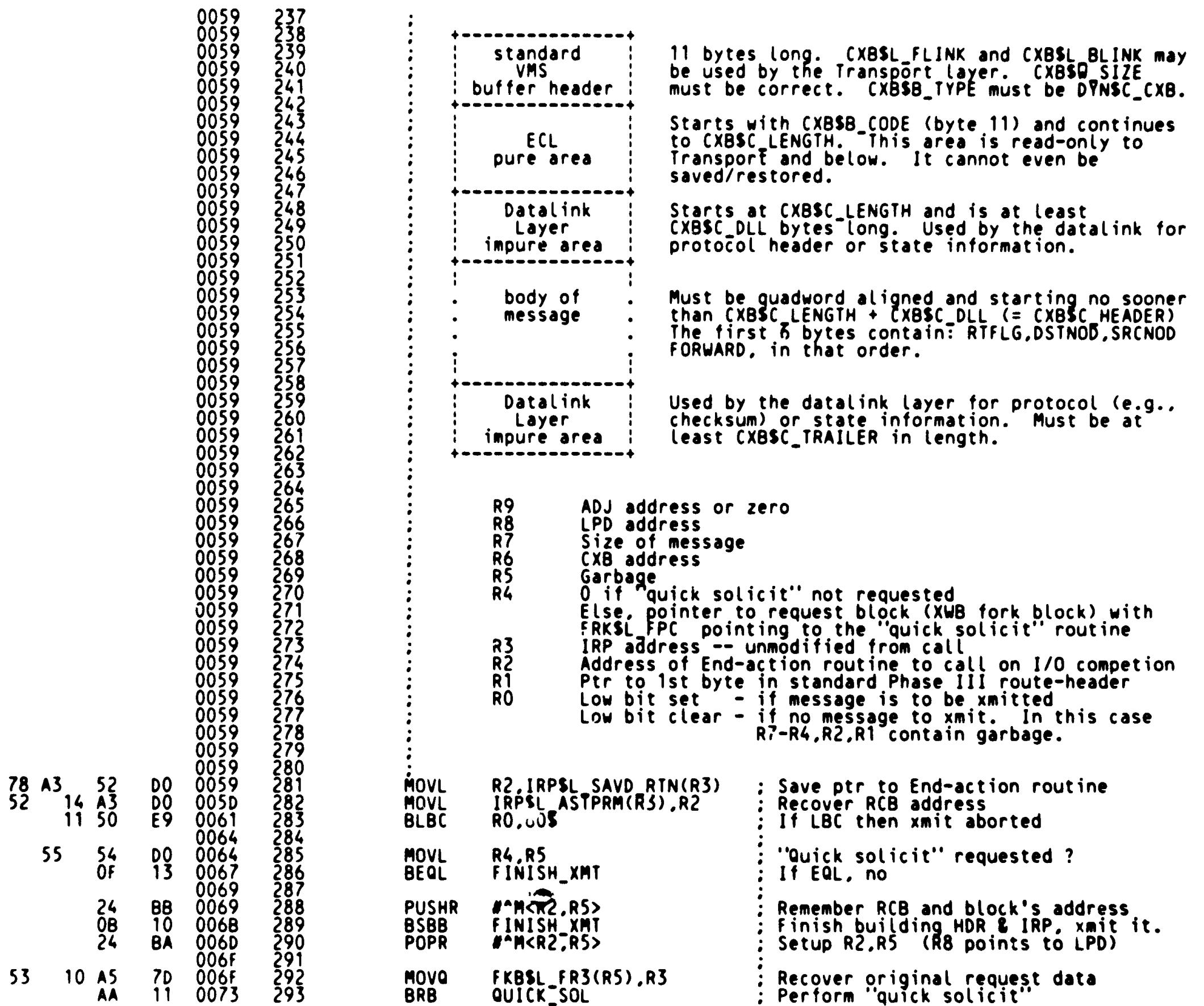
0000 44 .SBTTL MODIFICATION HISTORY
0000 45 :
0000 46 : AUTHOR: Alan D. Eldridge, CREATION DATE: 30-Oct-1983
0000 47 :
0000 48 : MODIFIED BY:
0000 49 :
0000 50 : V04-001 RNG0001 Rod Gamache 19-Mar-1984
0000 51 : Close off call to QRL\$SETUP_CHAN.
0000 52 :
0000 53 :
0000 54 :

```
0000 56 .SBTTL DECLARATIONS
0000 57 :
0000 58 : INCLUDE FILES:
0000 59 :
0000 60 $CXBDEF
0000 61 $DYNDEF
0000 62 $FKBDEF
0000 63 $IPLDEF
0000 64 $IRPDEF
0000 65 $IODEF
0000 66 $SSDEF
0000 67 $TQEDEF
0000 68 $UCBDEF
0000 69 $VADEF
0000 70
0000 71 $ADJDEF
0000 72 $LPDDEF
0000 73 $RCBDEF
0000 74
0000 75 $NETSYMDEF
0000 76 $NETUPDDEF
0000 77 $NSPMMSGDEF
0000 78
0000 79 $CXBEXTDEF          ; NETDRIVER CXB extensions
0000 80 $XWBDEF             ; XWB and LSB definitions
0000 81
0000 82 .iif ndf,IRPSQ_STATION, IRPSQ_STATION = 8+IRPSL_MEDIA
0000 83
0000 84
```

```
0000 86
0000 87;
0000 88: LOCAL DEFINITIONS
0000 89:
0000000F 0000 90 HSZ_DELTA = TR4$C_HSZ_DATA-TR3$C_HSZ_DATA ; Difference in header sizes
00000008 0000 91
00000008 0000 92 MAX_C_LPE = 8 ; Max LPE's
00000008 0000 93
00000008 0000 94
00000008 0000 95
00000000 0000 96 LPESQ_IRP_WAIT = 0 ; Listhead of waiting processes
00000008 0000 97 LPESQ_IRP_FREE = 8 ; Listhead of free IRP's
00000010 0000 98 LPESB_IRP_CNT = 16 ; Count of current IRP's
00000014 0000 99 LPESC_LENGTH = 20 ; Round up the length
00000001 0000 100
00000001 0000 101: MACROS
00000001 0000 102
00000001 0000 103:
00000001 0000 104 CAS_MEASURE = 1 ;&
00000001 0000 105 .MACRO INC_PMS PMS_CELL ; Increment PMS cell
00000001 0000 106 .IF DF CAS_MEASURE
00000001 0000 107 .IF NE CAS_MEASURE
00000001 0000 108 .INCE G^PMSSGL_`PMS_CELL' ; Conditional assembly
00000001 0000 109 .ENDC ; Bump the counter
00000001 0000 110 .ENDC
00000001 0000 111 .ENDC
00000001 0000 112 .ENDC
00000001 0000 113 .ENDM INC_PMS ; .
00000000 0000 114
00000000 0000 115
00000000 0000 116
00000000 0000 117 .PSECT $SS115_DRIVER, LONG, EXE, RD, WRT ; Goto code PSECT
00000000 0000 118
00000000 0000 119
00000000 0000 120
```

0000 122 .SBTTL QRL\$SOLICIT - Process ECL request to xmit into the network
 0000 123 :+
 0000 124
 0000 125 An ECL (e.g. NSP) is requesting to xmit into the network. The request is
 0000 126 honored as soon as an IRP for the designated IRP is available.
 0000 127
 0000 128 INPUTS: R5 Fork block address
 0000 129 The FPC,FR3,FR4 fields are all scratch and must not
 0000 130 be modified by the caller until it is reactivated by
 0000 131 either QRL\$DENY or QRL\$GRANTED.
 0000 132 R4 ADJ index
 0000 133 R3 LPD i.d.
 0000 134 R2 RCB address
 0000 135 R1,R0 Scratch
 0000 136
 0000 137 (SP) Return address of caller
 0000 138 4(SP) Return address of caller's caller
 0000 139
 0000 140
 0000 141 OUTPUTS: See routines QRL\$GRANT or QRL\$DENY
 0000 142
 0000 143 -
 0000 144 QRL\$SOLICIT:: ; Process ECL request to xmit
 0000 145
 0000 146
 0000 147 Setup the fork block and pop the stack to simplify the code
 0000 148 in case the requestor needs to be suspended.
 0000 149
 0000 150
 0C A5 8ED0 0000 151 POPL FKB\$L_FPC(R5)
 07C0 8F BB 0004 152 PUSHR #^M<R6,R7,R8,R9,R10> : Save return addr, pop stack
 0008 153
 58 10 53 53 9A 0008 154 MOVZBL R3,R3 : Save regs
 28 B243 D0 000B 155 MOVQ R3,FB\$L_FR3(R5)
 05 10 0014 000F 156 MOVL @RC\$L_PTR_LPD(R2)[R3],R8 : Use only the index
 0016 157 BSBB 10\$: Save selection data
 07C0 8F BA 0016 158
 05 001A 159 POPR #^M<R6,R7,R8,R9,R10> : Get LPD address
 001B 160 RSB : Process request, okay to wait
 001B 161
 001B 162
 001B 163 10\$: ASSUME LPDSV_ACTIVE EQ 0 : Restore regs
 001B 164
 16 22 A8 E9 001B 165 BLBC LPDSW_STS(R8),QRL\$DENY : Done
 001F 166 QUICK_SOL:
 56 53 14 C5 001F 167 MULL3 #LPESC_LENGTH,R3,R6 : Br if no path to node
 00000000'GF CO 0023 168 ADDL G^NET\$RCB,R6 : Quick solicit entry
 002A 169
 002A 170
 002A 171 Get LPD specific IRP -- also serves as the 'input packet limiter'
 002A 172
 002A 173
 53 08 B6 0F 002A 174 REMQUE ALPESQ_IRP_FREE(R6),R3 : Get a free IRP
 11 1C 002E 175 BVC QRL\$GRANT : If VC then got one
 04 B6 65 0E 0030 176 INSLQUE (R5),ALPESQ_IRP_WAIT+4(R6)
 05 0034 177 RSB : Wait for IRP
 0035 178

0035 180 .SBTTL QRL\$DENY - Deny solicitor permission to transmit
 0035 181 .SBTTL QRL\$GRANT - Grant solicitor permission to transmit
 0035 182 :+
 0035 183 The RS fork process cannot be suspended beyond this point.
 0035 184
 0035 185
 0035 186
 0035 187 INPUTS: R9 Scratch
 0035 188 R8 LPD address
 0035 189 R7,R6 Scratch
 0035 190 R5 Fork block address
 0035 191 R4 ADJ index
 0035 192 R3 If QRL\$GRANT - IRP address
 0035 193 If QRL\$DENY - Scratch
 0035 194 R2 RCB address
 0035 195 R1,R0 Scratch
 0035 196
 0035 197
 0035 198 OUTPUTS: R7-R0 Garbage
 0035 199
 0035 200 All other registers are preserved.
 0035 201
 0035 202 :-
 0035 203 QRL\$DENY:
 8E 50 94 0035 204 CLRBL R0 : Deny permission to xmit
 OC B5 16 0037 205 MOVQ R2,(SP)+ : Indicate request denied
 52 8E 7D 003A 206 JSB AFKBSL_FPC(R5) : Save regs
 52 8E 7D 003D 207 MOVQ (SP)+,R2 : Tell requestor the bad news
 05 0040 208 RSB : Restore regs
 0041 209 : Done
 0041 210 QRL\$GRANT:
 0041 211 Call requestor back with:
 0041 212
 0041 213
 0041 214 R9 ADJ address
 0041 215 R8 LPD address
 0041 216 R7,R6 Scratch
 0041 217 R5 Fork block address
 0041 218 R4 Scratch
 0041 219 R3 IRP address only if R0 has low bit set, else scratch
 0041 220 R2 RCB address
 0041 221 R1 Scratch
 0041 222 R0 Low bit set if permission granted
 0041 223 : Low bit clear if permission denied
 0041 224
 0041 225
 59 2C B244 D0 0041 226 MOVL @RCBSL_PTR ADJ(R2)[R4],R9 : Get ADJ
 0046 227 :8 MOVW R10,IRPSQ_STATION+4(R3) : Store dest node addr
 40 A3 44 A3 04 A9 3C 0046 228 :8 BBC #ADJSV_RUN,ADJSB_STS(R9),10\$: If BC, "main" ADJ
 0046 229 :8 MOVZWL ADJSW_PNA(R9),IRPSQ_STATION+4(R3) : Set target address
 50 01 90 004B 230 10\$: MOVL #TR4SC_HIORD,IRPSQ_STATION(R3) : Say "okay to xmit"
 OC B5 16 0053 231 MOVB #1,R0 : Reactivate solicitor
 0056 232 JSB AFKBSL_FPC(R5)
 0059 233 :
 0059 234 :
 0059 235 : On return, the CXB and registers are setup as follows:
 0059 236 :



```

00B1 31 0075 294 60$: BRW      QRL$XMT_ABORTED      ; Recycle unused the IRP
0078 295
0078 296 FINISH_XMT:
0078 297
0078 298
0078 299
0078 300     . . . Journal the message to be transmitted
0078 301
0078 302
0078 303 . IF DF,JNX$$$ 
0078 304
0078 305 . PUSHL R0          ; Save registers
0078 306 . MOVL IRPSL_ASTPRM(R3),R2   ; Get RCB address
0078 307 . CLRL R0          ; Set journal type = Start xmt
0078 308 . BSBW TR_FILL_JNX    ; Store journal record
0078 309 . POPL R0          ; Restore registers
0078 310
0078 311 . ENDC
0078 312
0D 22 A8 07 E1 0078 313 BBC      #LPDSV_X25,LPDSW_STS(R8),100$ ; Skip if not X.25 datalink
007D 314
007D 315
007D 316     . . . X.25 circuits a CRC16 checksum on the data portion of the message.
007D 317
007D 318
0B BB 007D 319 PUSHR  #^M<R0,R1,R3> ; Save regs
52 50 D0 007F 320 :& CRC    CRC16,#0,R7,(R1) ; Calculate CRC16 on data
0B BA 0082 321 MOVL  R0,R2          ; Save CRC
0084 322 POPR  #^M<R0,R1,R3> ; Restore regs
71 52 B0 0084 324 MOVW  R2,-(R1) ; Save CRC in datagram
57 02 A0 0087 325 ADDW  #2,R7          ; Account
66 51 D0 008A 326 100$: MOVL  R1,(R6) ; Save address of start of data
0080 327
20 A3 20 B0 008D 328 MOVW  S^#IOS_WRITEBLK,IRPSW_FUNC(R3) ; Setup function
24 A3 56 D0 0091 329 MOVL  R6,IRPSL_IOSB(R3)    ; Buffer address into IOSB
0095 330
0095 331 ASSUME IRPSW_BOFF EQ 4+IRPSL_SVAPTE
0095 332
07 50 2C A3 9E 0095 333 MOVAB IRPSL_SVAPTE(R3),R0 ; Setup for auto-increment
22 A8 05 E1 0099 334 BBC    #LPDSV_XBF,LPDSW_STS(R8),120$ ; If BC, I/O is direct
009E 335
009E 336
009E 337     . . . Xmitter I/O is buffered
009E 338
009E 339
80 56 D0 009E 340 MOVL  R6,(R0)+ ; Setup buffer ptr in SVAPTE
80 B4 00A1 341 CLRW  (R0)+ ; Clear BOFF
19 11 00A3 342 BRB   140$ ; Continue
00A5 343 120$: . . .
00A5 344
00A5 345     . . . Xmitter I/O is direct
00A5 346
00A5 347
56 54 66 D0 00A5 348 MOVL  (R6),R4 ; Get msg address
56 54 00000000 GF D0 00A8 349 MOVL  G^MMGSGL_SPTBASE,R6 ; Get system page table base
51 15 09 EF 00AF 350 EXTZV #VASV_VPN,#VASS_VPN,R4,R1 ; Get Virtual page frame number

```

80	54	80	6641	DE	00B4	351	MOVAL	(R6)[R1],(R0)+	; Enter SVAPTE
				AB	00B8	352	BICW3	#^C<VASM_BYT>,R4,(R0)+	; Enter page offset into BOFF
				00BE	353	140\$:	:		
				00BE	354		:		
				00BE	355		Complete the IRP and queue it to the device		
				00BE	356				
				00BE	357				
				00BE	358		ASSUME IRPSW_BCNT EQ 2+IRPSW_BOFF		
				00BE	359		ASSUME IRPSL_BCNT EQ 0+IRPSW_BCNT		
				00BE	360				
	60	57	3C	00BE	361		MOVZWL R7,(R0)	; Enter BCNT	
		56	D4	00C1	362		CLRL R6	; Prevent buffer deallocation	
55	1C	A3	D0	00C3	363		MOVL IRPSL_UCB(R3),R5	; Get comm driver UCB	
	06	13	00C7	364			BEQL 150\$; If EQL then this is Local LPD	
00000000'GF		17	00C9	365			JMP G^EXESALTQUEPKT	; Send to "real" datalink	
			00CF	366					
			00CF	367	150\$:	BRW	TRSLOC_DLL_XMT	; Send to "local" datalink	
			00CF	368					
			00D3	369	150\$:	BUG_CHECK	NETNOSTATE,FATAL	; TRSLOC_DLL_XMT not global	
			00D3	370					
			00D3	371					

			00D3	373	QRL\$RTRN_X_10:			
07C0 8F	BB	00D3	374	DS8INT	#NETSC_IPL		: Xmt I/O completion	
		00D3	375	PUSHR	#^M<R6,R7,R8,R9,R10>		: Raise IPL	
		00D9	376	MOVL	IRPSL_ASTPRM(R5),R2		: Save regs	
52 14 A5	D0	00DD	377	MOVZBL	IRPSL_AST(R5),R0			
50 10 A5	9A	00E1	378	MOVL	@RCBS\$_PTR_LPD(R2)[R0],R8		: Get RCB pointer	
58 28 B240	D0	00E5	379				: Get LPD index	
		00EA	380				: Get LPD address	
		00EA	381					
		00EA	382	.IF	DF,JNX\$\$\$			
		00EA	383					
		00EA	384	MOVL	#8,R7		: Set length of IOSB	
		00EA	385	MOVAB	IRPSL_IOST1(R5),R1		: Journal the IOSB quadword	
		00EA	386	MOVB	#1,R0		: Journal type = xmt complete	
		00EA	387	BSBW	TR_FILL_JNX		; Store journal record	
		00EA	388					
		00EA	389	.ENDC				
		00EA	390					
50 24 A5	D0	00EA	391	MOVL	IRPSL_IOSB(R5),R0		: Get buffer	
24 A5	D4	00EE	392	CLRL	IRPSL_IOSB(R5)		: Detach it from the IRP	
		00F1	393					
		00F1	394					
		00F1	395					
		00F1	396					
		00F1	397					
		00F1	398					
		00F1	399					
		00F1	400					
		00F1	401					
		00F1	402					
		00F1	403					
		00F1	404					
		00F1	405					
		00F1	406					
		00F1	407					
		00F1	408					
		00F1	409					
		00F1	410					
		00F1	411					
		00F1	412					
		00F1	413					
		00F1	414					
78 B5	16	00F1	415	JSB	@IRPSL_SAVD_RTN(R5)			
		00F4	416	INCPMS	RCVBUFL	:& temp	; Deliver status to ECL layer	
0F 38 A5	E9	00FA	417	BLBC	IRPSL_IOST1(R5),30\$			
		00FE	418	BUMP	L,LPDSL_CNT_DPS(R8)			
		0107	419	INCPMS	DÉPLOCPR			
50 24 A5	D0	010D	420	30\$:	MOVL			
09 13	0111	421		BEQL	IRPSL_IOSB(R5),R0			
24 A5	D4	0113	422	CLRL	40\$			
00000000 GF	16	0116	423	JSB	IRPSL_IOSB(R5)			
53 55	D0	011C	424	40\$:	G^COMSDRVDEALMEM			
OC 10	011F	425		MOVL	R5,R3			
		0121	426	BSBB	QRL\$RTRN_X_IRP			
07C0 8F	BA	0121	427	POPR	#^M<R6,R7,R8,R9,R10>			
		0125	428	ENBINT				
		0128	429	RSB				

NETDRVQRL
V04-000

K 10
- DECnet 'Quick Routing Layer' module fo 16-SEP-1984 01:36:27 VAX/VMS Macro V04-00
QRL\$GRANT - Grant solicitor permission t 5-SEP-1984 02:20:21 [NETACP.SRC]NETDRVQRL.MAR;1 Page 11
(9)

0129 430

P - S S P I C P S P S P C A T 1 1 7 5 M - - - - - 2 T M

				0129	432	QRL\$XMT_ABORTED:		
				0129	433	MOVBL #1,IRPSL_IOST1(R3)		; User abort Xmit request ; Recycle IRP normally
				012D	434			
				012D	435	QRL\$RTRN_X_IRP:		
				012D	436	MOVZBL IRPSL_AST(R3),R0		; Recycle Xmt the IRP
				C5	437	MULL3 #LPESL_LENGTH,R0,R6		; Get LPD index
				CO	438	ADDL G^NETSQCB,R6		; Get LPE offset
				DO	439	MOVL IRPSL_ASTPRM(R3),R2		; Make it a pointer
					440			; Get RCB pointer
					441			
					442			
					443			
					444			
				OF	445	40\$: REMQUE ALPESQ_IRP_WAIT(R6),R5		; Get waiting process
				1D	446	BVS 70\$; If VS, none
				E9	447	BLBC IRPSL_IOST1(R3),50\$; If LBC, I/O was unsuccessful
				DO	448	MOVL FKB\$L_FR4(R5),R4		; Get ADJ index
				31	449	BRW QRL\$GRANT		; Reactivate the process
					450	50\$:		
					451			
					452			
					453			
					454			
					455			
					456			
					457			
					458			
					459			
					460	BSBW QRL\$DENY		; Reactivate the process
					461	BRB 40\$; Loop
					462	70\$: INSQUE (R3),ALPESQ_IRP_FREE+4(R6)		; Save IRP
					463	RSB		
					464			

```

015B 466 .SBTTL QRL$SETUP_CHAN - Setup channel to specified node
015B 467 ;+
015B 468
015B 469 INPUTS: R3 Non-zero LPD index
015B 470 R2 RCB pointer
015B 471 R1 Pointer to standard Phase III route-header
015B 472
015B 473 OUTPUTS: R4 ADJ index
015B 474 R3 Size of new route-header
015B 475 R1 Pointer to new route-header
015B 476 R0 LBS if successful, LBC otherwise
015B 477
015B 478 ;-
015B 479 QRL$SETUP_CHAN::: ; Setup channel to node
03F6 8F BB 015B 480 P0SHR #^M<R1,R2,R4,R5,R6,R7,R8,R9> ; Save regs
07 50 D4 015F 481 CLRL R0 ; Assume error
53 91 0161 482 CMPB R3,#MAX_C_LPE-1 ; Can we handle it?
0A 11 0164 483 ::88 BGEQU SS ; If GEQU, out of range
0164 484 BRB SS ; Always return failure
0166 485
0166 486
0166 487 ; Find ADJ and LPD
0166 488
0166 489
54 01 A1, 3C 0166 490 MOVZWL 1(R1),R4 ; Get remote node address
FE93. 30 016A 491 BSBW TRSGET-ADJ ; Get ADJ and LPD
03 50 E8 016D 492 BLBS R0,10$ ; If LBS okay
007C 31 0170 493 SS: BRW 100$ ; Exit
0173 494
76 58 50 D4 0173 495 10$: CLRL R0 ; & is the following needed?
72 59 1F E1 0175 496 BBC #31,R8,100$ ; Assume LPD or ADJ not there
50 2C A2 D0 017D 497 BBC #31,R9,100$ ; If BC, no LPD
80 59 D1 0181 498 MOVL RCB$L_PTR_ADJ(R2),R0 ; If BC, no ADJ
FB 12 0184 499 20$: CMPL R9,(R0)+ ; Address first ADJ pointer
50 2C A2 C2 0186 500 BNEQ 20$ ; This it ?
50 50 04 C6 018A 501 SUBL RCB$L_PTR_ADJ(R2),R0 ; If EQL, no
08 AE 50 01 C3 018D 502 DIVL #4,R0 ; Get difference in longwords
0192 503 SUBL3 #1,R0,8(SP) ; Convert to bytes
0192 504
0192 505 ; Save index R4 cell in stack
0192 506
0192 507
0192 508 ; Make sure LPE has IRP's. If LPE's don't exist, allocate them.
0192 509
56 00000000'GF D0 0192 510 MOVL G^NETSWCB,R6 ; Get LPE vector pointer
2C 12 0199 511 BNEQ 50$ ; If NEQ, it exits
51 AC 8F 9A 019B 512 MOVZBL #12+<LFESC_LENGTH*MAX_C_LPE>,R1 ; Setup length of LPE vector
FE5E. 30 019F 513 BSBW NET$ALONPGD_2 ; Allocate /zero the block
4A 50 E9 01A2 514 BLBC R0,100$ ; If LBC, nice try
56 52 0C C1 01A5 515 ADDL3 #12,R2,R6 ; Get address of vector area
00000000'GF 56 D0 01A9 516 MOVL R6,G^NETSWCB ; Setup LPE vector pointer
01B0 517
01B0 518 ASSUME LPESQ_IRP_FREE EQ 8+LPESQ_IRP_WAIT
01B0 519 ASSUME LPESC_LENGTH EQ 20
01B0 520
50 56 D0 01B0 521 MOVL R6,R0 ; Setup temp pointer
52 08 9A 01B3 522 MOVZBL #MAX_C_LPE,R2 ; Setup loop counter

```

60 50 DO 01B6 523 40\$:	MOVL R0,(R0)	; Setup first listhead
80 80 DE 01B9 524	MOVAL (R0)+,(R0)+	
60 50 DO 01BC 525	MOVL R0,(R0)	Setup second listhead
80 80 DO 01BF 526	MOVL (R0)+,(R0)+	
80 80 D5 01C2 527	TSTL (R0)+	Go to next LPE
EF 52 F5 01C4 528	SOBGTR R2,40\$	Loop
56 53 53 9A 01C7 530 50\$:	MOVZBL R3,R3	
56 53 14 C0 01CA 531	MULL3 #LPESC LENGTH,R3,R6	Use only the index portion
00000000'GF CO 01CE 532	ADDL G^NET\$QCB,R6	Get LPE offset
51 6E 7D 01D5 533	MOVQ (SP),R1	Make it a pointer
0099 30 01D8 534	BSBW QRL\$SETUP_X_IRP	Recover header ptr and RCB
11 50 E9 01DB 535	BLBC R0,100\$	Setup IRP's
011,E	;	If LBC, something's wrong
01DE	;	
51 6E 7D 01DE 541	MOVQ (SP),R1	
57 06 DO 01E1 542	MOVL #6,R7	Recover header ptr and RCB
0E 10 01E4 543	BSBB QRL\$SETUP_RTHDR	Standard header size
6E 51 DO 01E6 544	MOVL R1,(SP)	Setup the header
53 57 DO 01E9 545	MOVL R7,R3	Setup new header pointer
50 01 DO 01EC 546	MOVL #1,R0	Setup new header size
01EF	;	Say "success"
03F6 8F BA 01EF 548 100\$:	POPR #^M<R1,R2,R4,R5,R6,R7,R8,R9>	Restore regs
05 01F3 549	RSB	Return status in R0
01F4 550		

```

01F4 552 .SBTTL QRL$SETUP_RTHDR - Build route-header
01F4 553 :+
01F4 554
01F4 555 This routine converts the Phase III header passed by R1 to the proper format
01F4 556 according to the nature of the adjacency and the padding requirements of
01F4 557 the circuit.
01F4 558
01F4 559 INPUTS: R9 ADJ address
01F4 560 R8 LPD address
01F4 561 R7 Total number of bytes in message/header
01F4 562 R2 RCB address
01F4 563 R1 Pointer to start of Phase III route-header
01F4 564
01F4 565 OUTPUTS: R7 New message/header size
01F4 566 R4,R3 Garbage
01F4 567 R1 Pointer to start of new route-header
01F4 568 R0 Garbage
01F4 569
01F4 570 All other registers are preserved.
01F4 571
01F4 572 :-
01F4 573 QRL$SETUP_RTHDR: : Build/convert route-header
01F4 574
01F4 575
01F4 576 Build header based on output adjacency node type.
01F4 577
01F4 578 We will make a special check here, to see if we are an Endnode.
01F4 579 This is because on a BC circuit the "main" ADJ has a PTYPE of
01F4 580 "unknown" which prevents the building of a route header.
01F4 581
01F4 582 $DISPATCH RCB$B_ETY(R2),TYPE=B,-
01F4 583 <-
01F4 584 <ADJ$C_PTY_PH4N, 10$>,- ; Phase IV endnode
01F4 585 >
01FC 586 $DISPATCH ADJSB_PTYPE(R9),TYPE=B,-
01FC 587 <-
01FC 588 <ADJ$C_PTY_AREA 10$>,- ; Phase IV level 2 router
01FC 589 <ADJ$C_PTY_PH4 10$>,- ; Phase IV router
01FC 590 <ADJ$C_PTY_PH4N 10$>,- ; Phase IV endnode
01FC 591 <ADJ$C_PTY_PH3 30$>,- ; Phase III router
01FC 592 <ADJ$C_PTY_PH3N 30$>,- ; Phase III endnode
01FC 593 >
01FC 594
0200 595
0200 596
0200 597 All others including Phase II
0200 598
0200 599
57 06 C2 0200 600 SUBL #TR3$C_HSZ_DATA,R7 ; Adjust msg size
51 06 C0 0210 601 ADDL #TR3$C_HSZ_DATA,R1 ; Skip over Transport header
3E 11 0213 602 BRB 40$ ; Join common code
0215 603 10$: .
0215 604 .
0215 605 .
0215 606 .
0215 607 .
0215 608 ASSUME TR4$V_RTFLG_RTS EQ TR3$V_RTFLG_RTS

```

					0215 609	ASSUME TR4\$V_RTFLG_RQR EQ TR3\$V_RTFLG_RQR
					0215 610	
39 22 A8 0A E1 C3 CO	53 51 OF 0F	0215 611	BBC #LPDSV_BC,LPDSW_STS(R8),40\$; If BC, NOT a broadcast circuit			
	57 OF	021A 612	SUBL3 #HSZ_DELTA,R1,R3 ; Point to new header area			
		021E 613	ADDL #HSZ_DELTA,R7 ; Adjust msg size			
		0221 614				
		0221 615				
		0221 616	For Broadcast Circuits, always set the Intra-NI flag. It will be			
		0221 617	cleared by routers if they route this packet off the Ethernet.			
		0221 618				
		0221 619				
83 81 24 89		0221 620				
		0225 621	BISB3 #TR4\$M_RTFLG_INI!- ; Set the Intra-NI flag			
	54 81 B0	0225 622	TR4\$M_RTFLG_LNG,(R1)+,(R3)+ ; Set the long format flag			
	51 61 B0	0228 623	MOVW (R1)+,R4 ; Get destination address			
	83 B4	0228 624	MOVW (R1),R1 ; Get source node address			
83 000400AA 8F	83 54 80	022D 625	CLRW (R3)+ ; RESERVED D-AREA, D-SUBAREA			
	83 B4	0234 626	MOVL #TR4\$C_HIORD,(R3)+ ; Store destination HIORD			
83 000400AA 8F	83 51 80	0237 627	MOVW R4,(R3)+ ; Store destination address			
	83 D4	0239 628	CLRW (R3)+ ; RESERVED S-AREA, D-SUBAREA			
	51 EB A3 9E	0240 629	MOVL #TR4\$C_HIORD,(R3)+ ; Store source HIORD			
	08 11	0243 630	MOVW R1,(R3)+ ; Store source node address			
		0245 631	CLRL (R3)+ ; Clear NL2, VISIT-CT, SERVICE-CLASS and PROTOCOL TYPE			
		0248 632	MOVAB -TR4\$C_HSZ_DATA(R3),R1 ; Get new header pointer			
		0248 633	BRB 40\$; Join common code			
		0248 634 30\$:				
		0248 635				
		0248 636				
		0248 637				
		0248 638				
		0248 639				
		0248 640				
		0248 641				
		0248 642				
		0248 643				
		0248 644				
		0248 645				
		0248 646				
		0248 647				
01 A1 FCO0FC00 8F	CA	0248 648	BICL #TR4\$M_ADDR_AREA!<<TR4\$M_ADDR_AREA>>@16>,1(R1)			
		0253 649 40\$:				
		0253 650				
		0253 651				
		0253 652				
		0253 653				
03 22 A8 0D	53 51 D0 E1	0253 654	MOVL R1,R3			
	51 01 CA	0256 655	BBC #LPDSV_ALIGNW,LPDSW_STS(R8),60\$; If BC no word alignment needed			
03 22 A8 0E	E1 025E	656	BICL #1,R1 ; Else, backup to word boundary			
	51 07 CA	0263 657 60\$:	BBC #LPDSV_ALIGNQ,LPDSW_STS(R8),80\$; If BC no quad alignment needed			
	53 51 C2	0266 658	BICL #7,R1 ; Else, backup to quad boundary			
	08 13	0269 660	SUBL R1,R3 ; Calculate size of rounding			
	57 53 CO	0268 661	BEQL 100\$; Branch if no pad required			
61 53 80 8F	89 026E	662	ADDL R3,R7 ; Increase size of transfer			
	05 0273	663 100\$: RSB	BISB3 #^X<80>,R3,(R1) ; Set bit to indicate pad count			
		0274 664				

Phase III Router/Endnode

***** THE FOLLOWING IS A REQUIREMENT OF THE ARCHITECTURE *****

There are no known DECnet implementations which can handle node addresses from other areas. Therefore, for Phase III nodes we will always reset the area field of the source node address. There are checks in the route-thru code to prevent route-thru nodes from sending to Phase III nodes from other areas.

Pad the message if required

Copy start of message pointer

If BC no word alignment needed

Else, backup to word boundary

If BC no quad alignment needed

Else, backup to quad boundary

Calculate size of rounding

Branch if no pad required

Increase size of transfer

Set bit to indicate pad count

Done

```

0274 666 .SBTTL QRL$SETUP_X_IRP - Allocate, init, queue IRP
0274 667 +
0274 668
0274 669 INPUTS: R8 LPD address
0274 670 R6 LPE address
0274 671 R2 RCB address
0274 672
0274 673 OUTPUTS: R0 LBS if there are IRP's and the LPD is active
0274 674 R4,R3,R1 are clobbered
0274 675
0274 676
0274 677 All others are unchanged
0274 678
0274 679 -
0274 680 QRL$SETUP_X_IRP: ; Allocate, init, queue IRP
0274 681

      50 04 0274 682 CLRL R0 ; Assume error
      1C 22 A8 E9 0276 683 ASSUME LPDSV_ACTIVE EQ 0
      02 10 A6 91 0276 684 BLBC LPDSW_STS(R8),100$
      13 1E 027A 685 10$: CMPB LPESB_IRP_CNT(R6),#2
      15 10 0280 686 BGEQU 90$ ; If BC, inactive
      09 50 E9 0282 687 BSBBL SETUP_X_IRP ; Do we already have two ?
      10 A6 96 0285 688 BLBC R0,50$ ; If GEGU yes, that's enough
      OC B6 63 0E 0288 689 INCBL LPESB_IRP_CNT(R6)
      10 A6 95 028C 690 INSQUE (R3),BLPE$Q_IRP_FREE+4(R6) ; Do it
      EC 11 028C 691 :& INCWL RCBSW_TRANS(R2) ; If LBC, allocation failure
      03 13 0291 692 BRB 10$ ; Bump the count
      50 01 D0 0293 693 50$: TSTB LPESB_IRP_CNT(R6) ; Queue the IRP
      05 0296 694 BEQL 100$ ; Account for IRP
      0297 695 90$: MOVL #1,R0 ; Loop
      0297 696 100$: RSB Any IRP's ?
      0297 697 ; If EQL, return error
      0297 698 ; Indicate success
      0297 699 SETUP_X_IRP: ; Done
      24 BB 0297 700 PUSHR #^M<R2,R5> ; Save reqs
      51 C4 8F 9A 0299 701 MOVZBL #IRPSCL_LENGTH,R1 ; Setup IRP size
      00000000 GF 16 029D 702 JSB G^EXES$ALONONPAGED ; Get the block
      3C 50 E9 02A3 703 BLBC R0,200$ ; Br on error
      02A6 704
      02A6 705
      02A6 706 Zero the IRP and fill in selected fields
      02A6 707
      02A6 708
      62 00C4 8F 00 6E 52 DD 02A6 709 PUSHL R2 ; Save block address
      00 2C 53 8ED0 02A8 710 MOVC5 #0,(SP),#0,IRPSCL_LENGTH,(R2) ; Zero entire block
      02B0 02B3 711 POPL R3 ; Setup IRP pointer
      54 08 A3 9E 02B3 712 MOVAB IRPSW_SIZE(R3),R4 ; Advance to size field
      02B7 713
      02B7 714
      02B7 715
      02B7 716 ASSUME IRPSB_TYPE EQ 2+IRPSW_SIZE ; Enter size for deallocation
      02B7 717 ASSUME IRPSB_RMOD EQ 1+IRPSB_TYPE ; Enter buffer type and zero
      84 00C4 8F 80 02B7 718 MOVW #IRPSCL_LENGTH,(R4)+ ; RMOD to indicate "kernel"
      84 0A 98 02BC 719 MOVZBW S^#DYN$C_IRP,(R4)+ ; Assume IRPSL_PID EQ 1+IRPSB_RMOD
      02BF 720
      02BF 721
      02BF 722
  
```

		02BF	723	ASSUME	IRPSL_AST	EQ	4+IRPSL_PID	
		02BF	724	ASSUME	IRPSL_ASTPRM	EQ	4+IRPSL_AST	
		02BF	725	ASSUME	IRPSL_WIND	EQ	4+IRPSL_ASTPRM	
		02BF	726	ASSUME	IRPSL_UCB	EQ	4+IRPSL_WIND	
		02BF	727	ASSUME	LPDSL_UCB	EQ	4+LPDSL_WIND	
		02BF	728					
84	FE10	CF	9E	02BF	729	MOVAB	QRL\$RTRN X IO,(R4)+	: Enter return address into PID
84	20	A8	3C	02C4	730	MOVZWL	LPDSW_PTR(R8),(R4)+	: Enter LPD i.d. into AST
84	84	6E	D0	02C8	731	MOVL	(SP),TR4)+	: Enter RCB ptr into ASTPRM
84	OC	A8	7D	02CB	732	MOVQ	LPDSL_WIND(R8),(R4)+	: Enter WIND and UCB ptrs
		02CF	733					
		02CF	734	ASSUME	IRPSW_FUNC	EQ	4+IRPSL_UCB	
		02CF	735	ASSUME	IRPSB_EFN	EQ	2+IRPSW_FUNC	
		02CF	736	ASSUME	IRPSB_PRI	EQ	1+IRPSB_EFN	
		02CF	737	ASSUME	IRPSL_IOSB	EQ	1+IRPSB_PRI	
		02CF	738	ASSUME	IRPSW_CHAN	EQ	4+IRPSL_IOSB	
		02CF	739	ASSUME	IRPSW_STS	EQ	2+IRPSW_CHAN	
		02CF	740					
84	14	84	7C	02CF	741	CLRQ	(R4)+	: Clear FUNC,EFN,PRI,IOSB
03	22	A8	AE	02D1	742	MNEGW	LPDSW_CHAN(R8),(R4)+	: Enter CHAN
		64	B4	02D5	743	CLRW	(R4)	: Setup STS for direct I/O write
		64	05	E1	02D7	BBC	#LPDSV_XBF,LPDSW_STS(R8),100\$: If BC, writes are direct
		64	01	A8	02DC	BISW	#IRPSM_BUFIO,(R4)	: Setup for buffered I/O
		50	01	DO	02DF	747	100\$:	: and next reserved word
		24	BA	02E2	748	200\$:	MOVL #1,R0	: Indicate success
		05	02E4		749	POPR #^M<R2,R5>	: Recover regs	
		02E5	750		RSB		: Done	
		02E5	751					
		02E5	752					
		02E5	753	.END				

SS_NSPMSG	= 00000000		IRPSB_TYPE	= 0000000A
SS_TR3MSG	= 00000000		IRPSL_LENGTH	= 000000C4
SS_TR4MSG	= 00000000		IRPSL_AST	= 00000010
ACPSC_STA_F	= 00000004		IRPSL_ASTPRM	= 00000014
ACPSC_STA_H	= 00000005		IRPSL_BCNT	= 00000032
ACPSC_STA_I	= 00000000		IRPSL_IOSB	= 00000024
ACPSC_STA_N	= 00000001		IRPSL_IOST1	= 00000038
ACPSC_STA_R	= 00000002		IRPSL_PID	= 0000000C
ACPSC_STA_S	= 00000003		IRPSL_SAVD_RTN	= 00000078
ADJSB_PTYPE	= 00000001		IRPSL_SVAPTE	= 0000002C
ADJSC_PTY_AREA	= 00000003		IRPSL_UCB	= 0000001C
ADJSC_PTY_PH3	= 00000000		IRPSL_WIND	= 00000018
ADJSC_PTY_PH3N	= 00000001		IRPSM_BUFI0	= 00000001
ADJSC_PTY_PH4	= 00000004		IRPSQ_STATION	= 00000040
ADJSC_PTY_PH4N	= 00000005		IRPSW_BCN	= 00000032
ADJSW_PNA	= 00000004		IRPSW_BOFF	= 00000030
BUGS_NETNOSTATE	***** X 02		IRPSW_CHAN	= 00000028
CAS_MEASURE	= 00000001		IRPSW_FUNC	= 00000020
CNFS_ADVANCE	= 00000000		IRPSW_SIZE	= 00000008
CNFS_QUIT	= 00000002		IRPSW_STS	= 0000002A
CNFS_TAKE_CURR	= 00000003		LPDSL_CNT_DPS	= 00000042
CNFS_TAKE_PREV	= 00000001		LPDSL_UCB	= 00000010
COMSDRVDEALMEM	***** X 02		LPDSL_WIND	= 0000000C
CXB\$B_R_AREA	00000039		LPDSV_ACTIVE	= 00000000
CXB\$B_R_FLG	00000038		LPDSV_ALIGNQ	= 0000000E
CXB\$B_R_NSPTYP	00000039		LPDSV_ALIGNW	= 0000000D
CXB\$B_X_NSPTYP	0000004E		LPDSV_BC	= 0000000A
CXBSC_DLL	= 00000020		LPDSV_X25	= 00000007
CXBSC_HEADER	= 00000048		LPDSV_XBF	= 00000005
CXBSC_R_LENGTH	= 0000003C		LPDSW_CHAN	= 00000014
CXB\$L_R_MSG	0000002C		LPDSW_PTH	= 00000020
CXB\$L_R_RCB	00000028		LPDSW_STS	= 00000022
CXB\$T_DLL	= 00000028		LPESB_IRP_CNT	= 00000010
CXB\$T_X_DATA	00000057		LPESC_LENGTH	= 00000014
CXB\$T_X_XPORT	00000048		LPESQ_IRP_FREE	= 00000008
CXB\$W_R_ADJ	0000003A		LPESQ_IRP_WAIT	= 00000000
CXB\$W_R_BCN	00000030		LSB	= 00000000
CXB\$W_R_DSTNOD	00000034		LSB\$B_R_CXBCNT	= 00000028
CXB\$W_R_NSSEQ	0000003A		LSB\$B_R_CXBQUO	= 00000029
CXB\$W_R_PATH	00000032		LSB\$B_SPARE	= 0000002A
CXB\$W_R_SRCNOD	00000036		LSB\$B_STS	= 0000002B
CXB\$W_X_NSPACK	00000053		LSB\$B_X_ADJ	= 0000000B
CXB\$W_X_NSPLOC	00000051		LSB\$B_X_CXBACT	= 0000000D
CXB\$W_X_NSPREM	0000004F		LSB\$B_X_CXBCNT	= 0000000F
CXB\$W_X_NSSEQ	00000055		LSB\$B_X_CXBQUO	= 0000000E
DYNSC_IRP	= 0000000A		LSB\$B_X_PKTWND	= 0000000C
EXESA[ONONPAGED]	***** X 02		LSB\$B_X_REQ	= 0000000A
EXESA[LTQUEPKT]	***** X 02		LSB\$L_CROSS	= 0000002C
FINISH_XMT	00000078 R 02		LSB\$L_R_CXB	= 00000020
FKBSL_FPC	= 0000000C		LSB\$L_R_IRP	= 0000001C
FKBSL_FR3	= 00000010		LSB\$L_X_CXB	= 00000018
FKBSL_FR4	= 00000014		LSB\$L_X_IRP	= 00000014
HSZ_DELTA	= 0000000F		LSB\$L_X_PND	= 00000010
IOS_WRITEBLK	= 00000020		LSB\$M_BOM	= 00000020
IRPSB_EFN	= 00000022		LSB\$M_EOM	= 00000040
IRPSB_PRI	= 00000023		LSB\$M_LI	= 00000001
IRPSB_RMOD	= 0000000B		LSB\$S LSB	= 00000030

LSB\$S_SPARE	= 00000004	NSP\$C_HSZ_CI	= 000000F0
LSB\$S_STS	= 00000001	NSP\$C_HSZ_DATA	= 00000009
LSB\$V_BOM	= 00000005	NSP\$C_HSZ_DC	= 00000016
LSB\$V_EOM	= 00000006	NSP\$C_HSZ_DI	= 00000016
LSB\$V_LI	= 00000000	NSP\$C_HSZ_INT	= 00000009
LSB\$V_SPARE	= 00000001	NSP\$C_HSZ_LS	= 00000009
LSBSW_HAA	= 00000008	NSP\$C_INF_V31	= 00000001
LSBSW_HAR	= 00000006	NSP\$C_INF_V32	= 00000000
LSBSW_HAX	= 00000026	NSP\$C_INF_V33	= 00000002
LSBSW_HNR	= 00000024	NSP\$C_MAXRDR	= 00000009
LSBSW_HXS	= 00000004	NSP\$C_MAX_DELAY	= 00000014
LSBSW_LNX	= 00000002	NSP\$C_MAX_R_CXB	= 00000007
LSBSW_LUX	= 00000000	NSP\$C_MAX_XPW	= 00000007
MAX_C_LPE	= 00000008	NSP\$C_MSG_CA	= 00000024
MMG\$GC_SPTBASE	***** X 02	NSP\$C_MSG_CC	= 00000028
NET\$AL\$NP\$GD_Z	***** X 02	NSP\$C_MSG_CI	= 00000018
NET\$C_ACT_TIMER	= 0000001E	NSP\$C_MSG_DATA	= 00000000
NET\$C_EFN_ASYNC	= 00000002	NSP\$C_MSG_DC	= 00000048
NET\$C_EFN_WAIT	= 00000001	NSP\$C_MSG_DI	= 00000038
NET\$C_IPL	= 00000008	NSP\$C_MSG_DTACK	= 00000004
NET\$C_MAXACCFLD	= 00000027	NSP\$C_MSG_INT	= 00000030
NET\$C_MAXLINNAM	= 0000000F	NSP\$C_MSG_LIACK	= 00000014
NET\$C_MAXLNK	= 000003FF	NSP\$C_MSG_LS	= 00000010
NET\$C_MAXNODNAM	= 00000006	NSP\$C_SRV_MFC	= 00000002
NET\$C_MAXOBJNAM	= 0000000C	NSP\$C_SRV_NFC	= 00000000
NET\$C_MAX_AREAS	= 0000003F	NSP\$C_SRV_REQ	= 00000001
NET\$C_MAX_LINES	= 00000040	NSP\$C_SRV_SFC	= 00000001
NET\$C_MAX_NCB	= 0000006E	NSP\$M_ACK_NAK	= 0001000
NET\$C_MAX_NODES	= 000003FF	NSP\$M_ACK_NUM	= 0000FFF
NET\$C_MAX_OBJ	= 000000FF	NSP\$M_ACK_VALID	= 0008000
NET\$C_MAX_WQE	= 00000014	NSP\$M_DATA_BOM	= 00000020
NET\$C_MINBUFSIZ	= 000000C0	NSP\$M_DATA_EOM	= 00000040
NET\$C_TID_ACT	= 00000003	NSP\$M_DATA_OVFW	= 00000080
NET\$C_TID_RUS	= 00000001	NSP\$M_FLW_CHAN	= 0000000C
NET\$C_TID_XRT	= 00000002	NSP\$M_FLW_DRV	= 000000F0
NET\$C_TRCTL_CEL	= 00000002	NSP\$M_FLW_INT	= 00000020
NET\$C_TRCTL_OVR	= 00~0005	NSP\$M_FLW_INUSE	= 00000010
NET\$C_UTLBUFSIZ	= 00001000	NSP\$M_FLW_LISUB	= 00000004
NET\$M_MAXLNKMSK	= 000003FF	NSP\$M_FLW_MODE	= 00000003
NET\$WCB	***** X 02	NSP\$M_FLW_SP1	= 00000008
NSP\$\$\$QUAL_ACK	= 00000000	NSP\$M_FLW_SP2	= 00000040
NSP\$\$\$QUAL_ALTFWL	= 00000000	NSP\$M_FLW_SP3	= 00000080
NSP\$\$\$QUAL_DATA	= 00000000	NSP\$M_FLW_XOFF	= 00000001
NSP\$\$\$QUAL_FLW	= 00000000	NSP\$M_FLW_XON	= 00000002
NSP\$\$\$QUAL_INF	= 00000000	NSP\$M_INF_VER	= 00000003
NSP\$\$\$QUAL_MSG	= 00000000	NSP\$M_MSG_INT	= 00000020
NSP\$\$\$QUAL_SRV	= 00000000	NSP\$M_MSG_LI	= 00000010
NSP\$C_EXT_LNK	= 0000001E	NSP\$M_SRV_01	= 00000003
NSP\$C_FLW_DATA	= 00000000	NSP\$M_SRV_EXT	= 00000080
NSP\$C_FLW_INT	= 00000001	NSP\$M_SRV_FLW	= 0000000C
NSP\$C_FLW_NOP	= 00000000	NSP\$M_SRV_REQ	= 000000F3
NSP\$C_FLW_XOFF	= 00000001	NSP\$M_SRV_SP1	= 00000070
NSP\$C_FLW_XON	= 00000002	NSP\$R_QUAL	= 00000000
NSP\$C_HSZ_ACK	= 00000007	NSP\$\$ACK_NUM	= 0000000C
NSP\$C_HSZ_CA	= 00000003	NSP\$\$ACK_SP2	= 00000002
NSP\$C_HSZ_CC	= 00000064	NSP\$\$DATA_SP	= 00000005
NSP\$C_HSZ_CD	= 000000F0	NSP\$\$FLW_CHAN	= 00000002

NSP\$S_FLW_DRV	= 00000004		QUICK_SOL	= 0000001F R 02
NSP\$S_FLW_MODE	= 00000002		RCB\$B_ETY	= 0000008A
NSP\$S_INF_VER	= 00000002		RCB\$L_PTR_ADJ	= 0000002C
NSP\$S_MSG_SP1	= 00000004		RCB\$L_PTR_LPD	= 00000028
NSP\$S_NSPMSG	= 00000005		SETUP_X_IRP	= 00000297 R 02
NSP\$S_QUAL	= 00000005		SIZ..	= 00000001
NSP\$S_QUAL_ACK	= 00000002		TRSC_MAXHDR	= 0000001C
NSP\$S_QUAL_ALTFW	= 00000001		TRSC_NI_ALLEND1	= 040000AB
NSP\$S_QUAL_DATA	= 00000001		TRSC_NI_ALLEND2	= 00000000
NSP\$S_QUAL_FLW	= 00000001		TRSC_NI_ALLROU1	= 030000AB
NSP\$S_QUAL_INF	= 00000001		TRSC_NI_ALLROU2	= 00000000
NSP\$S_QUAL_MSG	= 00000005		TRSC_NI_PREFIX	= 000400AA
NSP\$S_QUAL_SRV	= 00000001		TRSC_NI_PROT	= 00000360
NSP\$S_SRV_01	= 00000002		TRSC_PRI_ECL	= 0000001F
NSP\$S_SRV_FLW	= 00000002		TRSC_PRI_RTHRU	= 0000001F
NSP\$S_SRV_SP1	= 00000003		TRSGET_ADJ	***** X 02
NSP\$V_ACK_NAK	= 0000000C		TR3\$\$\$QUAL_MSG	= 00000000
NSP\$V_ACK_NUM	= 00000000		TR3\$\$\$QUAL_RTFLG	= 00000000
NSP\$V_ACK_SP2	= 0000000D		TR3\$C_RSZ_DATA	= 00000006
NSP\$V_ACK_VALID	= 0000000F		TR3\$C_MSG_DATA	= 00000002
NSP\$V_DATA_BOM	= 00000005		TR3\$C_MSG_HELLO	= 00000005
NSP\$V_DATA_EOM	= 00000006		TR3\$C_MSG_INIT	= 00000001
NSP\$V_DATA_OVFW	= 00000007		TR3\$C_MSG_NOP2	= 00000008
NSP\$V_DATA_SP	= 00000000		TR3\$C_MSG_ROUT	= 00000007
NSP\$V_FLW_CHAN	= 00000002		TR3\$C_MSG_STR2	= 00000058
NSP\$V_FLW_DRV	= 00000004		TR3\$C_MSG_VERF	= 00000003
NSP\$V_FLW_INT	= 00000005		TR3\$M_MSG_CTL	= 00000001
NSP\$V_FLW_INUSE	= 00000004		TR3\$M_MSG_RTH	= 00000002
NSP\$V_FLW_LISUB	= 00000002		TR3\$M_RTFC[G_PH2	= 00000040
NSP\$V_FLW_MODE	= 00000000		TR3\$M_RTFLG_RQR	= 00000008
NSP\$V_FLW_SP1	= 00000003		TR3\$M_RTFLG RTS	= 00000010
NSP\$V_FLW_SP2	= 00000006		TR3\$R_QUAL	= 00000000
NSP\$V_FLW_SP3	= 00000007		TR3\$\$QUAL	= 00000001
NSP\$V_FLW_XOFF	= 00000000		TR3\$\$QUAL_MSG	= 00000001
NSP\$V_FLW_XON	= 00000001		TR3\$\$QUAL_RTFLG	= 00000001
NSP\$V_INF_VER	= 00000000		TR3\$\$RTFLG 012	= 00000003
NSP\$V_MSG_INT	= 00000005		TR3\$\$TR3MSG	= 00000001
NSP\$V_MSG_LI	= 00000004		TR3\$V_MSG_CTL	= 00000000
NSP\$V_MSG_SP1	= 00000000		TR3\$V_MSG_RTH	= 00000001
NSP\$V_SRV_01	= 00000000		TR3\$V_RTFC[G_012	= 00000000
NSP\$V_SRV_EXT	= 00000007		TR3\$V_RTFLG 5	= 00000005
NSP\$V_SRV_FLW	= 00000002		TR3\$V_RTFLG 7	= 00000007
NSP\$V_SRV_SP1	= 00000004		TR3\$V_RTFLG PH2	= 00000006
NSP\$W_DST[NK	= 00000001		TR3\$V_RTFLG_RQR	= 00000003
NSP\$W_SRCLNK	= 00000003		TR3\$V_RTFLG RTS	= 00000004
PMSSGC_DEPLOC PK	*****	X 02	TR4\$\$\$QUAL_ADDR	= 00000000
PMSSGL_RCVBUFFL	*****	X 02	TR4\$\$\$QUAL_RTFLG	= 00000000
PR\$ IPC	*****	X 02	TR4\$\$\$QUAL_SCLASS	= 00000000
QRL\$DENY	00000035 R	02	TR4\$C_BCE_MID1	= 040000AB
QRL\$GRANT	00000041 R	02	TR4\$C_BCE_MID2	= 00000000
QRL\$RTRN_X_IO	000000D3 R	02	TR4\$C_BCR_MID1	= 030000AB
QRL\$RTRN_X_IRP	0000012D R	02	TR4\$C_BCR_MID2	= 00000000
QRL\$SETUP_CHAN	00000158 RG	02	TR4\$C_BCT3MULT	= 00000008
QRL\$SETUP_RTHDR	000001F4 R	02	TR4\$C_END_NODE	= 00000003
QRL\$SETUP_X_IRP	00000274 R	02	TR4\$C_HIORD	= 000400AA
QRL\$SOLICIT	00000000 RG	02	TR4\$C_HSZ_DATA	= 00000015
QRL\$XMT_ABORTED	00000129 R	02	TR4\$C_MSG_BCEHEL	= 0000000D

TR4\$C_MSG_BCRHEL	= 0000000B	XWBSC_COMLNG	= 000000A4
TR4\$C_MSG_LDATA	= 00000006	XWBSC_CONLNG	= 0000112
TR4\$C_MSG_RUATA	= 00000002	XWBSC_DATA	= 00000010
TR4\$C_PRO_TYPE	= 00000360	XWBSC_LOGIN	= 00000040
TR4\$C_RTR_LVL1	= 00000002	XWBSC_LPRNAM	= 00000014
TR4\$C_RTR_LVL2	= 00000001	XWBSC_NDC_LNG	= 00000020
TR4\$C_T3MOLT	= 00000002	XWBSC_NUMSTA	= 00000008
TR4\$C_VER_HIB	= 00000000	XWBSC_RID	= 00000010
TR4\$C_VER_LOWW	= 00000002	XWBSC_RPRNAM	= 00000014
TR4\$M_ADDR_AREA	= 0000FC00	XWBSC_STA_CAR	= 00000002
TR4\$M_ADDR_DEST	= 000003FF	XWBSC_STA_CCS	= 00000004
TR4\$M_RTFLGINI	= 00000020	XWBSC_STA_CIR	= 00000003
TR4\$M_RTFLGLNG	= 00000004	XWBSC_STA_CIS	= 00000001
TR4\$M_RTFLGRQR	= 00000008	XWBSC_STA_CLO	= 00000000
TR4\$M_RTFLGRTS	= 00000010	XWBSC_STA_DIR	= 00000006
TR4\$R_QUAL	= 00000000	XWBSC_STA_DIS	= 00000007
TR4\$S_ADDR_AREA	= 00000006	XWBSC_STA_RUN	= 00000005
TR4\$S_ADDR_DEST	= 0000000A	XWBSL_DEA_IRP	= 0000104
TR4\$S_QUAL	= 00000002	XWBSL_FPC	= 00000020
TR4\$S_QUAL_ADDR	= 00000002	XWBSL_FR3	= 00000024
TR4\$S_QUAL_RTFLG	= 00000001	XWBSL_FR4	= 00000028
TR4\$S_QUAL_SCLASS	= 00000001	XWBSL_ICB	= 000010C
TR4\$S_RTFLG_01	= 00000002	XWBSL_IRP_ACC	= 00000080
TR4\$S_RTFLG_VER	= 00000002	XWBSL_LINR	= 0000002C
TR4\$S_SCLASS_57	= 00000003	XWBSL_ORGUCB	= 00000010
TR4\$S_TR4MSG	= 00000002	XWBSL_PID	= 00000034
TR4\$V_ADDR_AREA	= 0000000A	XWBSL_VCB	= 00000030
TR4\$V_ADDR_DEST	= 00000000	XWBSL_WLBL	= 00000004
TR4\$V_RTFLG_01	= 00000000	XWBSL_WLFL	= 00000000
TR4\$V_RTFLGINI	= 00000005	XWB\$M_FLG_BREAK	= 00000001
TR4\$V_RTFLGLNG	= 00000002	XWB\$M_FLG_CLO	= 0000200
TR4\$V_RTFLGRQR	= 00000003	XWB\$M_FLG_IAVL	= 0001000
TR4\$V_RTFLGRTS	= 00000004	XWB\$M_FLG_SCD	= 0000100
TR4\$V_RTFLGVER	= 00000006	XWB\$M_FLG_SDACK	= 00000008
TR4\$V_SCLASS_1	= 00000001	XWB\$M_FLG_SDFL	= 0004000
TR4\$V_SCLASS_57	= 00000005	XWB\$M_FLG_SDT	= 00000080
TR4\$V_SCLASS_BC	= 00000004	XWB\$M_FLG_SIACK	= 00000004
TR4\$V_SCLASS_LS	= 00000002	XWB\$M_FLG_SIFL	= 0002000
TR4\$V_SCLASS_METR	= 00000000	XWB\$M_FLG_SLI	= 00000010
TR4\$V_SCLASS_SUBA	= 00000003	XWB\$M_FLG_TBPR	= 00000800
VASM_BYTE	= 00001FF	XWB\$M_FLG_WBP	= 00000040
VASS_VPN	= 00000015	XWB\$M_FLG_WBUF	= 00000002
VASV_VPN	= 00000009	XWB\$M_FLG_WDAT	= 00000400
XWB	= 00000000	XWB\$M_FLG_WHGL	= 00000020
XWB\$B_ACCESS	= 00000008	XWB\$M_PRO_CCA	= 00000008
XWB\$B_DATA	= 00000058	XWB\$M_PRO_NAR	= 00000010
XWB\$B_FIPL	= 0000001F	XWB\$M_PRO_NFC	= 00000001
XWB\$B_LOGIN	= 000000CC	XWB\$M_PRO_PH2	= 00000004
XWB\$B_LPRNAM	= 000000A4	XWB\$M_PRO_SFC	= 00000002
XWB\$B_PRO	= 0000005A	XWB\$M_STS_ASTPND	= 00000400
XWB\$B_RID	= 0000006F	XWB\$M_STS_ASTREQ	= 00000800
XWB\$B_RPRNAM	= 000000B8	XWB\$M_STS_CON	= 00000010
XWB\$B_SP3	= 0000006E	XWB\$M_STS_DIS	= 00000C8
XWB\$B_STA	= 0000001E	XWB\$M_STS_DTNAK	= 00000100
XWB\$B_TYPE	= 0000000A	XWB\$M_STS_LINAK	= 00000200
XWB\$B_X_FLW	= 0000006C	XWB\$M_STS_NDC	= 0001000
XWB\$B_X_FLWCNT	= 0000006D	XWB\$M_STS_OVF	= 00000080

XWB\$M_STS_RBP	= 00000040	XWB\$V_STS_CON	= 00000004
XWB\$M_STS_SOL	= 00000004	XWB\$V_STS_DIS	= 00000003
XWB\$M_STS_TID	= 00000001	XWB\$V_STS_DTNAK	= 00000008
XWB\$M_STS_TLI	= 00000002	XWB\$V_STS_LINAK	= 00000009
XWB\$M_STS_TMO	= 00000020	XWB\$V_STS_NDC	= 0000000C
XWB\$Q_FORK	= 00000014	XWB\$V_STS_OVF	= 00000007
XWB\$Q_FREE_CXB	= 00000118	XWB\$V_STS_RBP	= 00000006
XWB\$R_CON_BLK	= 000000A4	XWB\$V_STS_SOL	= 00000002
XWB\$R_RUN_BLK	= 000000A4	XWB\$V_STS_TID	= 00000000
XWB\$S	= 00000006	XWB\$V_STS_TLI	= 00000001
XWB\$S_COMLNG	= 0000006E	XWB\$V_STS_TMO	= 00000005
XWB\$S_CON_BLK	= 0000006E	XWB\$W_CI_PATH	= 00000110
XWB\$S_DATA	= 00000010	XWB\$W_DECAY	= 0000004E
XWB\$S_DT	= 00000030	XWB\$W_DLY_FACT	= 00000056
XWB\$S_FLG	= 00000002	XWB\$W_DLY_WGHT	= 00000058
XWB\$S_FORK	= 00000008	XWB\$W_ELAPSE	= 0000004A
XWB\$S_FREE_CXB	= 00000008	XWB\$W_FLG	= 0000001C
XWB\$S_LI	= 00000030	XWB\$W_LOCLNK	= 0000003E
XWB\$S_LOGIN	= 0000003F	XWB\$W_LOCSIZ	= 00000040
XWB\$S_LPRNAM	= 00000013	XWB\$W_PATH	= 00000038
XWB\$S_NDC	= 00000020	XWB\$W_PROGRESS	= 00000052
XWB\$S_PRO	= 00000001	XWB\$W_REFCNT	= 0000000C
XWB\$S RID	= 00000010	XWB\$W_REMLNK	= 0000003C
XWB\$S_RPRNAM	= 00000013	XWB\$W_REMNOD	= 0000003A
XWB\$S_RUN_BLK	= 00000064	XWB\$W_REMSIZ	= 00000042
XWB\$S_STS	= 00000002	XWB\$W_RETRAN	= 00000054
XWB\$S_XWB	= 00000120	XWB\$W_R_REASON	= 00000044
XWB\$T	= 00000112	XWB\$W_SIZE	= 00000008
XWB\$T_DATA	= 0000005C	XWB\$W_STS	= 0000000E
XWB\$T_DT	= 000000A4	XWB\$W_TIMER	= 00000050
XWB\$T_LI	= 000000D4	XWB\$W_TIM_ID	= 00000048
XWB\$T_LOGIN	= 000000CD	XWB\$W_TIM_INACT	= 0000004C
XWB\$T_LPRNAM	= 000000A5	XWB\$W_X_REASON	= 00000046
XWB\$T_RID	= 00000070	XWB\$Z_NDC	= 00000084
XWB\$V_FLG_BREAK	= 00000000		
XWB\$V_FLG_CLO	= 00000009		
XWB\$V_FLG_IAVL	= 0000000C		
XWB\$V_FLG_SCD	= 00000008		
XWB\$V_FLG_SDACK	= 00000003		
XWB\$V_FLG_SDFL	= 0000000E		
XWB\$V_FLG_SDT	= 00000007		
XWB\$V_FLG_SIACK	= 00000002		
XWB\$V_FLG_SIFL	= 0000000D		
XWB\$V_FLG_SLI	= 00000004		
XWB\$V_FLG_TBPR	= 0000000B		
XWB\$V_FLG_WBP	= 00000006		
XWB\$V_FLG_WBUF	= 00000001		
XWB\$V_FLG_WDAT	= 0000000A		
XWB\$V_FLG_WHGL	= 00000005		
XWB\$V_PRO_CCA	= 00000003		
XWB\$V_PRO_NAR	= 00000004		
XWB\$V_PRO_NFC	= 00000000		
XWB\$V_PRO_PH2	= 00000002		
XWB\$V_PRO_SFC	= 00000001		
XWB\$V_STS_ASTPND	= 0000000A		
XWB\$V_STS_ASTREQ	= 0000000B		

```
+-----+
! Psect synopsis !
+-----+
```

PSECT name	Allocation	PSECT No.	Attributes														
.ABS .	00000000 (0.)	00 (0.)	NOPIC	USR	CON	ABS	LCL	NOSHR	NOEXE	NORD	NOWRT	NOVEC	BYTE				
\$ABSS	00000057 (87.)	01 (1.)	NOPIC	USR	CON	ABS	LCL	NOSHR	EXE	RD	WRT	NOVEC	BYTE				
SSS115_DRIVER	000002E5 (741.)	02 (2.)	NOPIC	USR	CON	REL	LCL	NOSHR	EXE	RD	WRT	NOVEC	LONG				

```
+-----+
! Performance indicators !
+-----+
```

Phase	Page faults	CPU Time	Elapsed Time
Initialization	33	00:00:00.09	00:00:01.29
Command processing	152	00:00:01.04	00:00:05.78
Pass 1	524	00:00:20.74	00:00:55.10
Symbol table sort	0	00:00:03.61	00:00:07.15
Pass 2	142	00:00:03.86	00:00:09.29
Symbol table output	65	00:00:00.47	00:00:01.41
Psect synopsis output	4	00:00:00.03	00:00:00.03
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	922	00:00:29.84	00:01:20.05

The working set limit was 2000 pages.

115222 bytes (226 pages) of virtual memory were used to buffer the intermediate code.

There were 120 pages of symbol table space allocated to hold 2276 non-local and 41 local symbols.

753 source lines were read in Pass 1, producing 15 object records in Pass 2.

57 pages of virtual memory were used to define 39 macros.

```
+-----+
! Macro library statistics !
+-----+
```

Macro library name	Macros defined
\$255\$DUA28:[SHRLIB]NMALIBR.MLB;1	0
\$255\$DUA28:[SHRLIB]EVDEF.MLB;1	0
\$255\$DUA28:[NETACP.OBJ]NETDRV.MLB;1	3
\$255\$DUA28:[NETACP.OBJ]NET.MLB;1	7
\$255\$DUA28:[SYS.OBJ]LIB.MLB;1	11
\$255\$DUA28:[SYSLIB]STARLET.MLB;2	8
TOTALS (all libraries)	29

2504 GETS were required to define 29 macros.

There were no errors, warnings or information messages.

MACRO/LIS=LISS:NETDRVQRL/OBJ=OBJ\$S:NETDRVQRL MSRC\$S:NETDRVQRL/UPDATE=(ENHS:NETDRVQRL)+EXECMLS/LIB+LIB\$S:NET/LIB+LIB\$S:NETDRV/LIB+SHRLIB\$

0277 AH-BT13A-SE
VAX/VMS V4.0

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